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SSI 32H6810A/6810B
5V Servo & Motor Speed Drivers

May 1994

DESCRIPTION

The SSI 32H6810A/6810B Servo/MSC Drivers, a CMOS monolithic integrated circuit housed in a 48-lead TQFP package, operates from a single 5V supply. It provides a fully integrated servo driver and a spindle motor commutator with internal power FETs. The servo driver is intended for use in disk drive head positioning systems employing linear or rotary voice coil motors. The commutator in conjunction with a microprocessor (μP) or digital signal processor (DSP), provides a complete spindle motor speed control system. The device is ideal for use in 5V small-form disk drive applications.

FEATURES

- **48-lead TQPF package**
- **Internal 1A Servo/MSC drivers**
- **NMOS output stage, no blocking diodes required**
- **No deadband, low distortion, class-B output for Servo driver**
- **Gain select switch for a wide dynamic range of servo inputs**
- **Optimal commutation delay without external components or Hall sensors**
- **Reduced dv/dt on commutation - no snubber networks required**
- **Unipolar and Bipolar modes for MSC driver**
- **Multiple Brake/Retract modes**
- **Internal precision voltage reference**
- **Power fault detection with built-in retract circuitry**
- **Thermal overload protection**
- **Low power CMOS design with Sleep mode**

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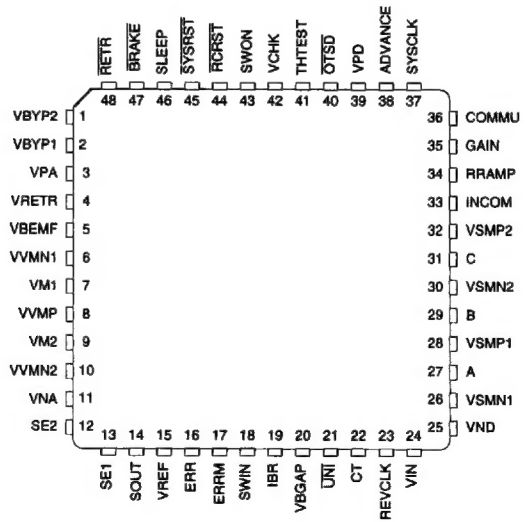
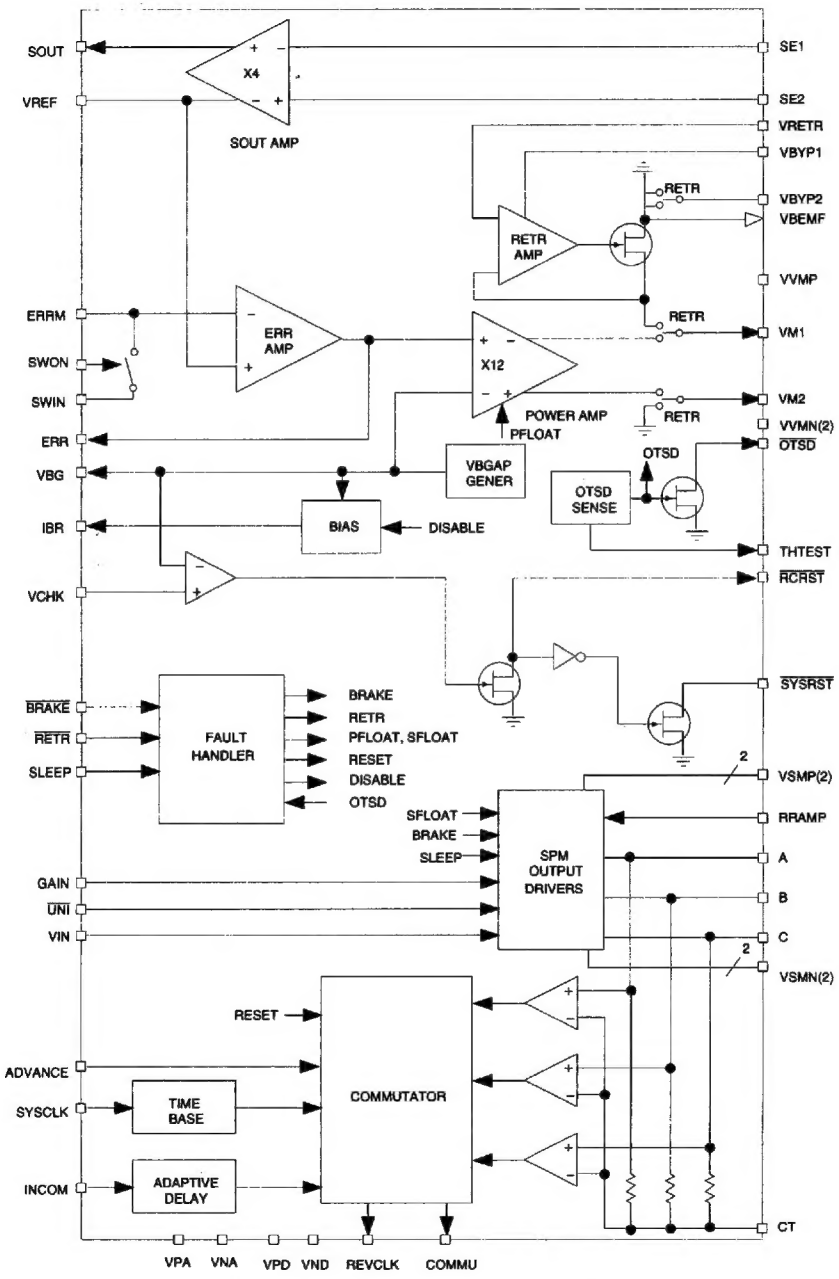
PIN DIAGRAM



48-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.



BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION

As shown in the block diagram, the SSI 32H6810A/6810B can be divided into three major sections: servo positioner, spindle motor commutator/driver, control circuitry.

SERVO POSITIONER

The servo positioner is a power transconductance amplifier for use in driving a voice coil servo motor (VCM). It has two primary modes of operation, normal (or linear) and retract. The retract mode is activated by a power supply failure or upon an external command per Table 2. Otherwise the device operates in linear mode. The servo positioner consists of SOUT amplifier, ERR amplifier, retract amplifier, power amplifier.

SOUT Amplifier

The SOUT amplifier generates a voltage at SOUT, proportional to positioner current, by sensing the voltage across an external resistor, Rs, amplifying and referencing to VREF. Since the common mode voltage on Rs can range over the full power supply, while the differential voltage is in the order of millivolts, the SOUT amplifier is realized with a high input common mode rejection and low input offset.

ERR Amplifier

The ERR amplifier is a high gain op amp. Due to the fixed gain of the power amp, ERR is proportional to the VCM voltage. The negative input of this amplifier is the system summing junction for the currents which are proportional to the desired VCM current, the measured VCM current, and the VCM voltage.

Power Amplifier

The power amplifier is a fixed gain voltage amplifier with differential inputs and outputs. Its input is the differential voltage between ERR and VBG. Its output drives the VCM directly through an internal NMOS bridge. An internal charge pump generates gate voltages higher than VVMP so the upper NMOS devices can drive VM1 and VM2 up to VVMP. Class B operation is guaranteed by a crossover protection circuitry, which ensures that only one NMOS in each leg of the H-bridge is active.

Retract Amplifier

When a voltage fault is sensed or upon an external command, the servo positioner enters into retract mode. In this mode, it is assumed that no current is available from VVMP. Thus power for this mode comes from VBEMF, from the rectified spindle back emf voltage, and from VBYP1, a voltage generated from the external storage capacitor C_{BYP}. The retract amplifier is powered by VBYP1. It senses the voltage at VRETR and, through a power NMOS source follower, raises VM1 to VRETR. The drain of the source follower is VBEMF.

SPINDLE MOTOR COMMUTATOR/DRIVER

The spindle motor commutator in conjunction with external components provides the motor driving capability for starting, accelerating and rotational speed regulation for brushless DC motors without the need for Hall sensors. Its control is accomplished via ADVANCE, $\overline{\text{RETR}}$, $\overline{\text{BRAKE}}$, SLEEP, GAIN, $\overline{\text{UNI}}$, and INCOM and its operation is monitored via COMMU, REVCLK. The speed regulation control loop is completed with a µP or DSP external to this device.

Commutator

Motor armature position is determined by monitoring the coil voltage of the winding that is not presently being driven by the drivers. The back emf from the coil, in conjunction with the state of the output drivers, indicates the armature position. The back emf is compared with a reference at CT and initiates commutation "events" when the appropriate comparison is made. Commutation is the sequential switching of drive current to the motor windings. Because the back emf comparison event occurs prior to the time when optimum commutation should occur, it is preferred to delay commutation by a predetermined time after the comparison. The commutation delay is provided by a circuitry that measures the interval between comparison events and delays commutation by a time equal to 3/7 of the prior measured interval. The circuit is adaptive and will provide the optimum delay for a wide range of motor speeds (-80% to 50% of the nominal value). Since the commutation of motor coils typically causes transients, the commutation delay circuit also provides a noise blanking function that prevents the circuit from responding back emf comparison events for a period of time equal to 4/7 of the interval between events after the comparison event. The commutation table is described in Table 1.

Motor speed control may be accomplished by measuring the period of the output signal at COMMU.

SPINDLE MOTOR COMMUTATOR/DRIVER (continued)

Transconductance Amplifier

Input pin VIN is the non-inverting input of a transconductance amplifier that uses the lower driver transistor, that is presently active per the commutation state, as the power driver element. An external resistor is used to sense the current flowing through the drive transistor source (and hence the motor coil current). The voltage across the sense resistor is amplified by a gain stage (Av = 5 or 10 selected by the GAIN pin) and fed to the inverting input of the transconductance output stage.

Power Amplifier

The output pins A, B and C are intended to drive motor coils directly. The output drivers operate to reduce switching noise transients by limiting dv/dt during commutation. Each output consists of two N-channel MOSFET drivers, one for pull-up to VSMP and one for pull-down to VSMN. The pull-up FET functions as a switch with voltage rise and fall times of about 25 µs. The pull-down FET is a part of the transconductance amplifier that converts the voltage VIN into motor current (Imotor = VIN/(RSENSE • Av), where Av is either 5 or 10). When the pull-down output is commutating to the off state, dv/dt on the respective pin is controlled such that dv/dt is approximately 15/RRAMP volts per µs, where RRAMP is measured in kohms.

Motor Start-up

Motor starting is accomplished by a companion µP or DSP via ADVANCE, SLEEP, $\overline{\text{BRAKE}}$ and COMMU. The commutation counter is reset to state 0 during power-up or upon a µP command asserting SLEEP high. Once it has been reset to this known state 0, the commutation counter can then be incremented by one with each rising edge of subsequent ADVANCE pulses. A typical start-up begins with $\overline{\text{BRAKE}}$ low (by asserting $\overline{\text{RETR}}$ low to ensure the servo head is retracted and the spindle motor is in stationary), SLEEP high (to reset the commutation counter to state 0), and ADVANCE high (to exclude internal commutations), then follows with $\overline{\text{BRAKE}}$ high and SLEEP low. Up to this time, the commutation counter will be state 0, but the lower driver output B remains inactive to prevent current from flowing through the motor (out of A that is high). At the first rising edge of subsequent ADVANCE pulses, the commutation state 1 is selected and the drivers are per Table 1. Note that ADVANCE at logic high excludes internal commutations. COMMU provides feedback to the µP on motor activity.

CONTROL CIRCUITRY

The control circuitry consists of a power fault detector, a thermal overload circuit, and control logic. The inputs to the control circuitry are VCHK, SLEEP, $\overline{\text{RETR}}$, and $\overline{\text{BRAKE}}$, along with the internal signals from the thermal overload detector.

The power fault detector monitors the system power supply Vdd to prevent the VCM driver from responding to a false command during a power failure. The system power supply is applied at VCHK through an external resistor divider and compared with an internal voltage reference at VBG. When a power failure is sensed, the $\overline{\text{SYSRST}}$ is asserted low and the retract mode is activated.

The thermal overload circuit monitors the die temperature to prevent an excessive current flowing through VCM or SPM drivers. If the die temperature exceeds approximately 135°C, the $\overline{\text{OTSD}}$ is asserted low and both drivers are turned off. The drivers will become operative after the temperature is reduced and the ADVANCE is asserted high.

Seven operating modes are selected via SLEEP, $\overline{\text{RETR}}$ and $\overline{\text{BRAKE}}$ (when the system power supply is present) per Table 2. If the system power supply is not present (VCHK<VBG), power for the braking circuitry during retract and spin-down is provided by the charge stored on an external capacitor on VBYP1, power for the retract circuitry is provided by the back emf voltage at VBEMF and the retract circuitry itself is driven by the charge stored on the capacitor between VBPY1 and VBYP2.

STATE	COMMU	Pull-Downs A	B	C	Pull-Ups A	B	C
0, (Reset state)	0	off	on (1)	off	on	off	off
1	1	off	off	on	on	off	off
2	0	off	off	on	off	on	off
3	1	on	off	off	off	on	off
4	0	on	off	off	off	off	on
5	1	off	on	off	off	off	on
(1) B is off in reset state, see text.							

TABLE 1: Commutation States

VCHK>VBGAP	SLEEP	$\overline{\text{BRAKE}}$	$\overline{\text{RETR}}$	MODE	ANALOG	VCM DRIVER	SPM DRIVER
0	X	1	X	Power Fault	On	Retract	Float
0	X	0	X	Power Fault	On	Retract	Low Z to GND
1	1	1	1	Sleep	Off	Float	Float
1	1	0	1	Sleep/Brake	Off	Float	Low Z to GND
1	1	0	0	Sleep/Retract	Off	Retract	Low Z to GND
1	1	1	0	Sleep/Retract	Off	Retract	Float
1	0	0	X	Brake/Retract	On	Retract	Low Z to GND
1	0	1	0	Retract (Spindle Run)	On	Retract	Active
1	0	1	1	Run	On	Active	Active
X	X	X	X	Thermal Shutdown	On	Float	Float

TABLE 2: Operating Mode Control

NOTES:
1. $\overline{\text{BRAKE}}$ internally linked to force retract.
2. Voltage fault circuit is never turned off.
3. Counter is reset when sleep input is high.

The circuit also provides an over temperature detection function. If the die temperature exceeds 135°C (approximately), $\overline{\text{OTSD}}$ is asserted low and all output drivers are turned off. The drivers will become operative after the temperature is reduced and ADVANCE is asserted high.

Whenever the VCM driver is either in retract or flat, the device is in Power-Saver mode where all VCM analog circuits are turned off except the retract amplifier. (6810B only)

PIN DESCRIPTION

POWER SUPPLIES

NAME	TYPE	DESCRIPTION
VPA	I	Supply: Analog positive power supply.
VNA	I	Ground: Analog ground.
VPD	I	Supply: Digital positive power supply.
VND	I	Ground: Digital ground. VND is circuitry ground and also the low side input to the current SENSE amplifier and thus care should be taken to see that VND and the low side of the external Rsense resistor are at the same potential.
VVMP	I	Supply: Positve supply for voice coil motor.
VVMN1, VVMN2	I	Supply: Negative supply for voice coil motor.

POSITIONER

SWON	I	Analog switch control input. When active high, it turns on the analog switch between ERRM and SWIN.
SWIN	I	Analog switch, the other side of the switch is connected to ERRM.
SOUT	O	The current sense amplifier output. SOUT is referenced to VREF.
ERR	O	The error amplifier output. ERR is used to provide compensation to the transconductance loop. ERR is referenced to VBGAP.
ERRM	I	The error amplifier inverting input.
VREF	I	The reference voltage for the error amplifier and the current sense amplifier. An external bypass capacitor of 0.1 µF may be added from this pin to ground to filter out its high-frequency noise.
VRETR	I	The retract voltage. If left open, the retract voltage will be the default setting. This value can be over-ridden by biasing VRETRACT externally.
VM1	O	Connection for voice coil motor.
VM2	O	Connection for the other side of voice coil motor.
SE1, SE2	I	The voltage across the sense resistor for the voice motor current.

MOTOR SPEED CONTROL

SYSCLK	I	System clock (input) pin. SYSCLK is 2 MHz nominal and is used to generate internal timing signals.
COMMU	O	Commutation count pin. COMMU is the LSB of the commutation counter.
REVCLK	O	REVCLK is COMMU divided by six.
$\overline{\text{UNI}}$	I	Unipolar mode (inverse) select pin. This pin will turn all upper drivers off when low. Pulled high internally to provide the default bipolar mode.

MOTOR SPEED CONTROL (continued)

NAME	TYPE	DESCRIPTION
ADVANCE	I	Advance pin. ADVANCE is controlled by microprocessor during start mode to increment the commutation counter. The rising edge of ADVANCE will increment the counter. ADVANCE held high will inhibit internal incrementing of the counter, ADVANCE held low permits the normal operation of commutation from back-emf events.
INCOM	I	Commutation delay control. Adaptive commutation delay may be adjusted from its nominal value of 3/7 of the commutation interval by sinking or sourcing current from this pin. It is recommended that INCOM pin be pulled high during start-up. (32H6810A only)
VIN	I	Control Voltage input pin. The internal driver transistors and internal predriver circuits form a transconductance amplifier which will set motor current in relation to VIN. In conjunction with Rsense at VSMN input and the gain of the Sense amplifier, transconductance (Gm) = Im/VIN = 1/ (Rsense • gain), gain = 5,10.
A, B, C	O	Motor Drive Outputs. These pins provide drive to the motor coils.
CT	I	Back EMF input from motor coil center tap. Input connected to the center tap for sensing generated back emf voltages. It is also derived internally from A, B, C through a resistor network (y-connection).The circuit uses the back-emf voltages to determine rotor position and effect commutation.
RRAMP	I	Lower driver turn-off dv/dt setting resistor. External resistor from VPD to this pin sets the dv/dt slope of the motor coil voltage when the lower drivers are commutating to the off state. The dv/dt is approximately given by the relationship: dv/dt = 15/RRAMP, where dv/dt is expressed in volts/μs and RRAMP in kΩ. A typical value for RRAMP is 200 kΩ.
GAIN	I	Sense amplifier gain control pin. In normal operation, this pin is tied to high to set sense amplifier gain = 5. In low motor current operation, amplifier gain = 10 can be set by tying this input to low.
VSMP1,VSMP2	I	Supply: Positive supply for spindle motor.
VSMN1, VSMN2	I	Supply: Negative for spindle motor. Current monitoring sense amplifier (high side) input pin and motor current returns to ground. **All pins must be connected with low resistance circuit board traces.** The lower driver transistor current (hence motor current) comes out of these pins to Rsense resistor to monitor motor current. During normal (at speed) operation, the circuit will control the voltage across this resistor (multiplied by the gain of the sense amplifier) to match VIN.
		VVMP, VVMN, VSMP and VSMN conductors must be sized in accordance with anticipated motor current. The analog and digital supplies should be bypassed separately. VPA and VPD should be shorted externally, VNA and VND should be shorted externally.

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PIN DESCRIPTION (continued)

MISCELLANEOUS

NAME	TYPE	DESCRIPTION
VBYP1	I	The bypassed power supply. An external voltage for BRAKE and RETRACT circuitry. An external capacitor is attached to this pin and an internal circuit will charge this pin to VCC. The charge on this capacitor is used by the brake and retract function when VCC is removed (power-off). The capacitor must hold sufficient charge during the period when VCC is lost while retract is taking place (20 to 50 ms) so it will have enough voltage to drive the outputs during braking. Very little current is used during power-off braking so that C can be chosen from the retract conditions: $C \geq Tretract \bullet Ivbyp\ (Float\ mode)/.5V$ or approximately: $C \geq 40E\text{-}6 \bullet Tretract$ This pin is normally a diode drop below VPA, rising by VBEMF during retract.
VBYP2	I	The other side of the bypass capacitor connection. This pin is normally at VNA, rising to VBEMF during retract.
VBEMF	I	Rectified spindle back emf voltage. This input provides current to the internal retract power amplifier.
SLEEP	I	Sleep pin. When asserted high, internal counters and registers are cleared. Refer to Table 2. Also forces an internal voltage fault which causes a head retract. Disables all output drivers, powers down all other circuitry except the over-temperature and voltage fault circuitry.
$\overline{RETR}$	I	Retract (inverse) pin. When asserted low, forces a retract. Refer to Table 2.
$\overline{BRAKE}$	I	Brake (inverse) pin. BRAKE is used to provide a delay between the initiation of fault-induced head retract and motor braking. A capacitor to ground and a resistor to SYSRST are selected such that $1.2 \bullet R \bullet C$ is equal to the maximum time required for retract. Refer to Table 2.
$\overline{OTSD}$	O	Thermal shutdown. When low, this open-collector output indicates that the junction temperature has exceeded the recommended operating range and the device is in thermal shutdown. In thermal shutdown, all output drivers are turned off and analog circuit de-biased.
VCHK	I	Comparator input for monitoring power supply. When VCHK goes below VBG, an internal voltage fault is generated and hence the servo head retract is activated.
VBGAP	O	Voltage reference at 2.23V, generated from the internal bandgap voltage, for use with the power supply monitor comparator.
IBR	O	A resistor is tied from this pin to ground to establish the bias current for internal circuitry.
$\overline{RCRST}$	I/O	This pin serves the dual purpose of providing power on reset and stretching short VFAULT pulses to a width suitable for the host microcontroller. An external RC network sets the minimum width of any SYSRST pulse. If $\overline{RCRST}$ is pulled low by external circuitry, this device will enter into the Retract mode and pull $\overline{SYSRST}$ low.
$\overline{SYSRST}$	O	When low, this open drain output indicates that an internal voltage fault has occured or that RCRST has been pulled low.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER		RATING
Supply voltage @ VPA, VPD, VVMP, VSMP	V_{DD}	-0.3 to 7V
Motor current @ VM1, VM2, A, B, C	I_{MAX}	-1 to 1A
Input voltage @	Vin	
CT, A, B, C, VBEMF, VBYP1, VBYP2		-0.3 to 12V
VM1,VM2,SE1,SE2		-0.3 to 7V
All other pins		-0.3 to Vdd+0.3V
Storage temperature	Tstg	-65 to 150°C
Lead temperature (10 sec duration)	T_{LEAD}	0 to 300°C
Maximum duration for SPM start-up current I_{SMP} = 1A @ T_A = 70°C	$T_{STARTUP}$	8 sec

RECOMMENDED OPERATING CONDITIONS

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply when the device is operated outside the recommended conditions.

Supply voltage @ VPA, VPD, VVMP, VSMP	Vdd	4.5 TO 5.5V
Supply current		
VPA+VPD		
Normal Mode	I_{DD}	20 mA
Power-Saver Mode (32H6810B only)	I_{PWSAV}	10 mA
Sleep Mode	I_{SLEEP}	2 mA
VVMP	I_{VMP}	0.4A
VSMP	I_{SMP}	0.8A
Input voltage @ VBEMF	VBEMF	1 to 10V
Input voltage @ VIN	VIN	0 to 2.5V
Input voltage @ VREF	VREF	0.5 to Vdd-2V
Input voltage @ VSMN	VSMN	0 to 0.5V
ADVANCE active low pulse width A/B		3/0.1 to 5/12 µs
Ambient temperature	T_A	0 to 70°C
Capacitive load on digital outputs	C_L	100 pF
Analog output load	C_L	50 pF
	R_L	10 kΩ
System clock		
Frequency	fc	1.5 to 2.5 MHz
Pulse Width	Twh, Twl	40 ns
Biasing resistor	Rbias	110 to 120 kΩ
External resistors	Rf, Rc	10 kΩ minimum

PERFORMANCE SPECIFICATIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Digital input ADVANCE, SYSCLK, $\overline{RETR}$,SLEEP, SWON, GAIN, $\overline{UNI}$	Vil		0.8			V
	Vih				2	V
Digital input @ $\overline{BRAKE}$	Vil		1.2			V
	Vih				2.4	V
Input leakage current @ ADVANCE, SYSCLK, $\overline{RETR}$, SLEEP, SWON, GAIN, $\overline{BRAKE}$, $\overline{RCRST}$			-1		1	µA
Input leakage current $\overline{UNI}$			-10		1	µA
Digital O/C output @ $\overline{RCRST}$, $\overline{SYSRST}$, $\overline{OTSD}$	Ioh	Voh = Vdd			1	µA
	Iol	Vol = 0.4 µA	4			mA
Digital output COMMU, REVCLK	Vol	Iol = 2 mA			0.4	V
	Voh	Ioh = -100 µA	2.4			V

SPINDLE MOTOR COMMUTATOR/DRIVER

Input leakage current @ VIN	0 < VIN < 2.5V	-1		1	µA
Total voltage drop across power FETs	Imotor = 0.5A			0.85	V
Rin @ A, B, C, CT while not driving	-0.3V < Vin < 7V	5			kΩ

SERVO POSITIONER

The following VCM performance specifications are measured with 16Ω resistive load and 0.5Ω sense resistor, unless otherwise noted.

VBYP1 current	Normal mode				100	µA
	Retract mode	Power off, VBYP1 = 3V			20	µA
	Brake mode	Power off, VBYP1 = 3V			10	µA
BEMF current	Normal mode	VBEMF = 4V			300	µA
	Retract mode	Power off, VBEMF = 3V VRETR = 0.5V, VBYP1 = 4V			20	µA
SOUT amplifier	Gain		3.9		4.1	V/V
	Input offset	SOUT = VREF	-3		3	mV
	Output swing	RL = 10 kΩ to VREF	0.15		Vdd - 1	V
ERR amplifier	Input offset		-15		15	mV
	Output swing		0.15		Vdd - 1.25	V
Power amplifier gain (VM1-VM2)/(ERR-VBG)			11		13	V/V

SERVO POSITIONER (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Total voltage drop across power FETs	Imotor = 0.2A			0.5	V
VCM transconductance		0.4		0.6	A/V
VCM bridge crossover time	Ivcm = 10 mA, peak step input			10	µs
VCM output THD	Ivcm = 0.1A, peak @ 100 Hz			2	%
SWIN on resistance				250	Ω
Retract amplifier (normal) VRETR leakage current		-1		1	µA
Retract amplifier (retract) Offset	VRETR = 0.1V, VBEMF > 1V	-100		0	mV
Maximum output current	VRETR = 0.5V, VM1 = VM2				
VBEMF = 1V	VBYP1 = 4.5V	60			mA
VBEMF = 1.5V		100			mA

CONTROL CIRCUITRY

VBG	Iout < +0.2mA	2.13		2.37	V
VCHK comparator offset		-15		15	mV
Thermal shutdown temperature threshold		125		145	°C

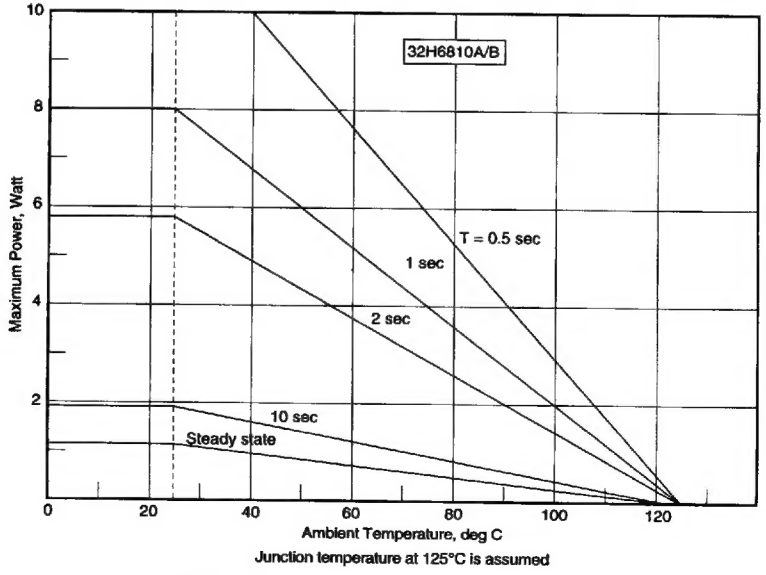
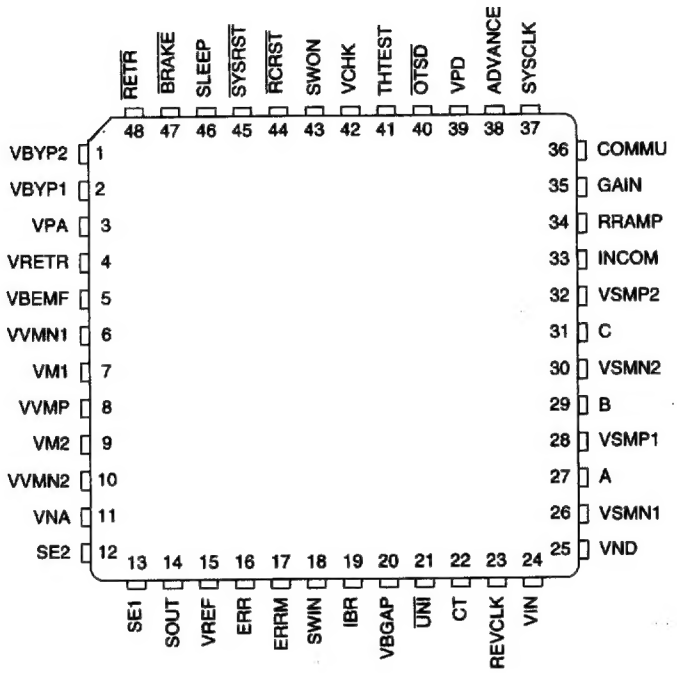


FIGURE 1: Power Dissipation Derating

SSI 32H6810A/6810B
5V Servo &
Motor Speed Drivers

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



48-Lead TQFP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PACKAGE MARK
SSI 32H6810A 48-Lead TQFP	32H6810A-CGT	32H6810A-CGT
SSI 32H6810B 48-Lead TQFP	32H6810B-CGT	32H6810B-CGT

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